



SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

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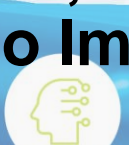
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SAMSUNG

Functional Accuracy Enhancement of In-House Virtual Platform using Commercial IP Model

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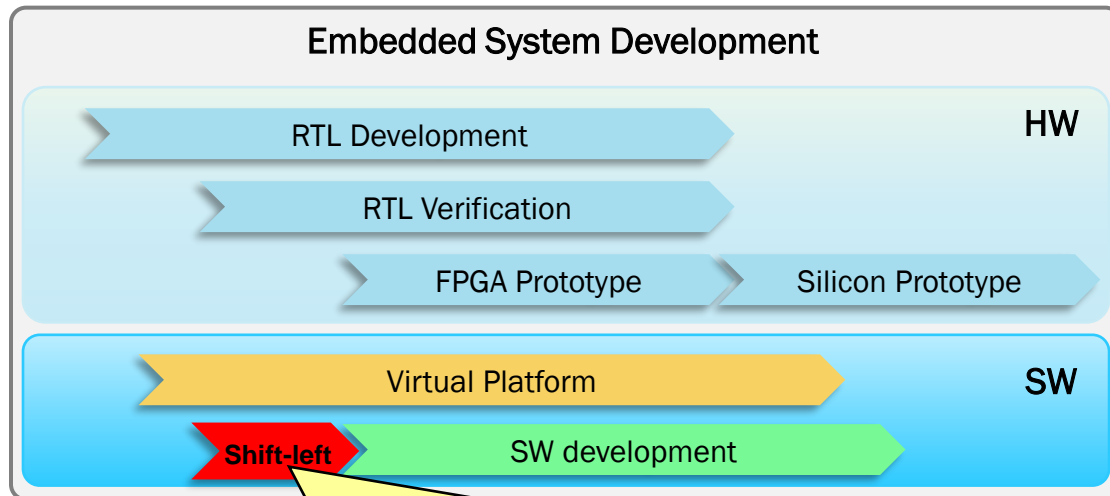


Outline

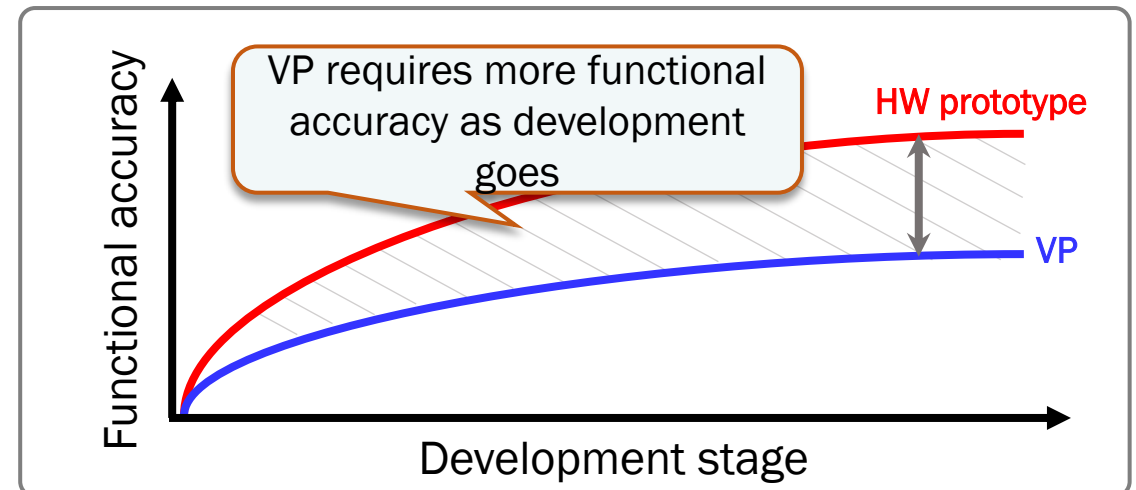
- Motivation
- Main idea: problem & solution
- Practical use
- Evidence
- Summary
- Reference

Motivation

- In conventional embedded SoC development, SW development schedule is determined by HW prototype.
- SW development based on virtual platform (VP) has been used in industrial field (e.g., SSD memory controller [1]).
 - (pros.) VP helps not only for shift-left of SW development, but also for improving SW quality through VP based CI/CD.
 - (cons.) VP has lower functional accuracy than that of HW prototype, because modeling 3rd party IP accurately requires considerable design knowledge and modeling effort.
- (*Motivation) In order to improve the functional accuracy, in-house VP needs to exploit the 3rd party IP (e.g., PCI express) model provided by commercial EDA, which required implementing a communication I/F for heterogeneous processes to integrate EDA IP model into in-house VP.

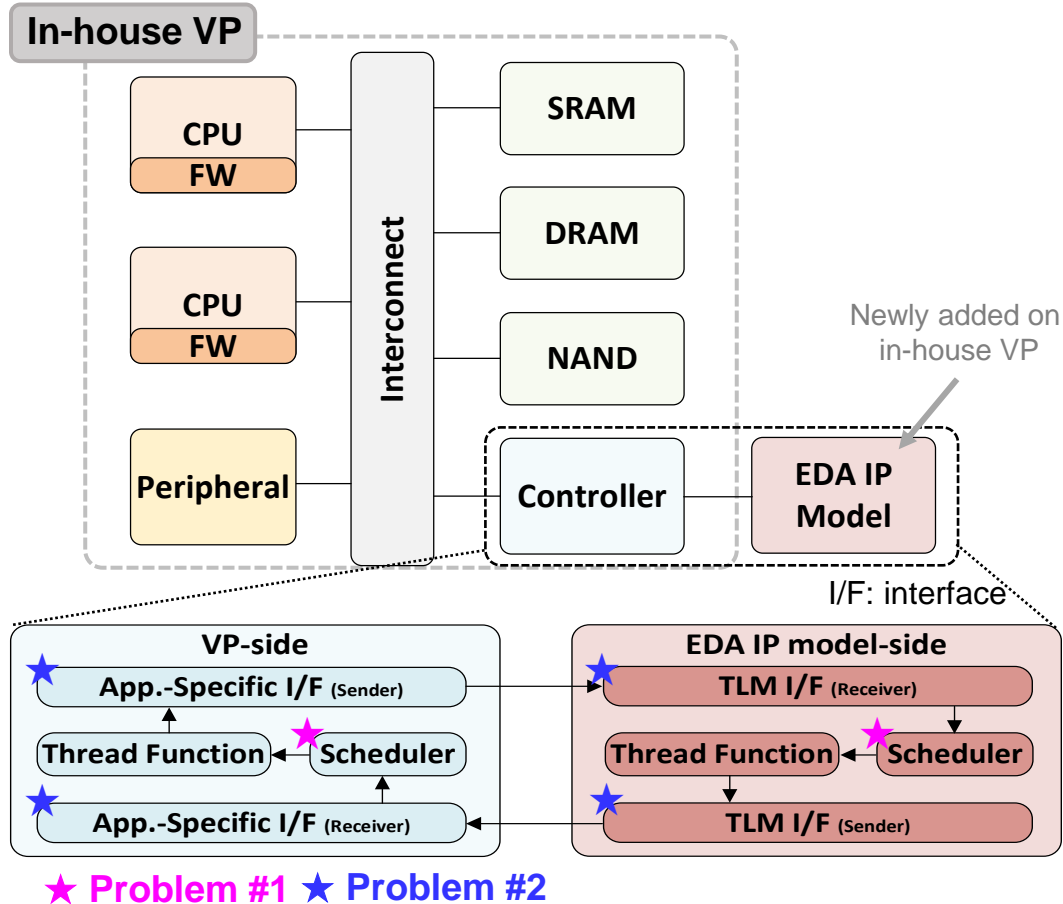


Gain from using a virtual platform



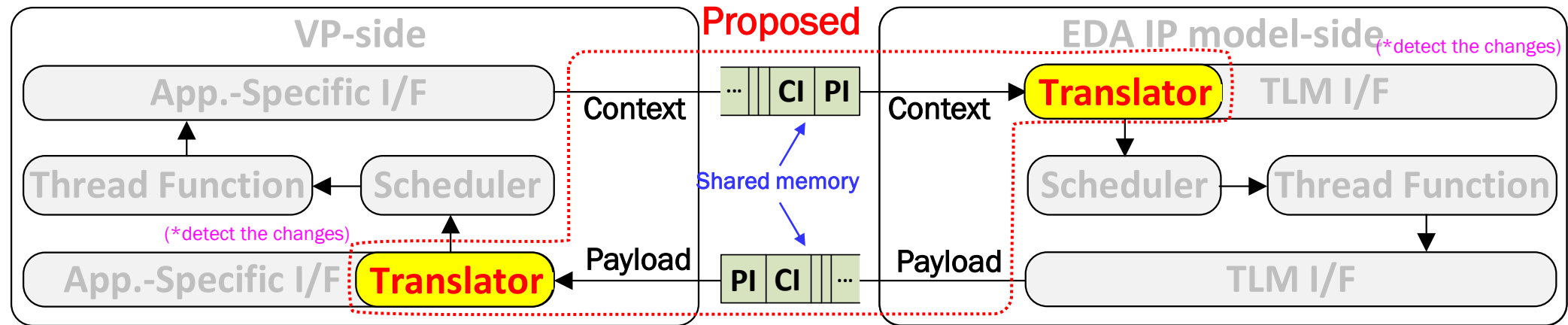
Main Idea: Problem

- When **EDA IP model (and the corresponding simulator)** is integrated to **in-house VP**, there are two main problems to solve.



- Problem #1:** Simulation synchronization between the two simulation processes (i.e., EDA IP and in-house VP)
 - ✓ The model status of EDA IP and VP are updated by each scheduler, respectively.
 - ✓ Communications between the two simulation processes must avoid interrupting each other scheduler's operation so that model status update is not affected by the communications.
- Problem #2:** Different data format between EDA IP model and in-house VP
 - ✓ Translation is required on both I/Fs (i.e., Application-Specific and TLM).

Main Idea: Solution



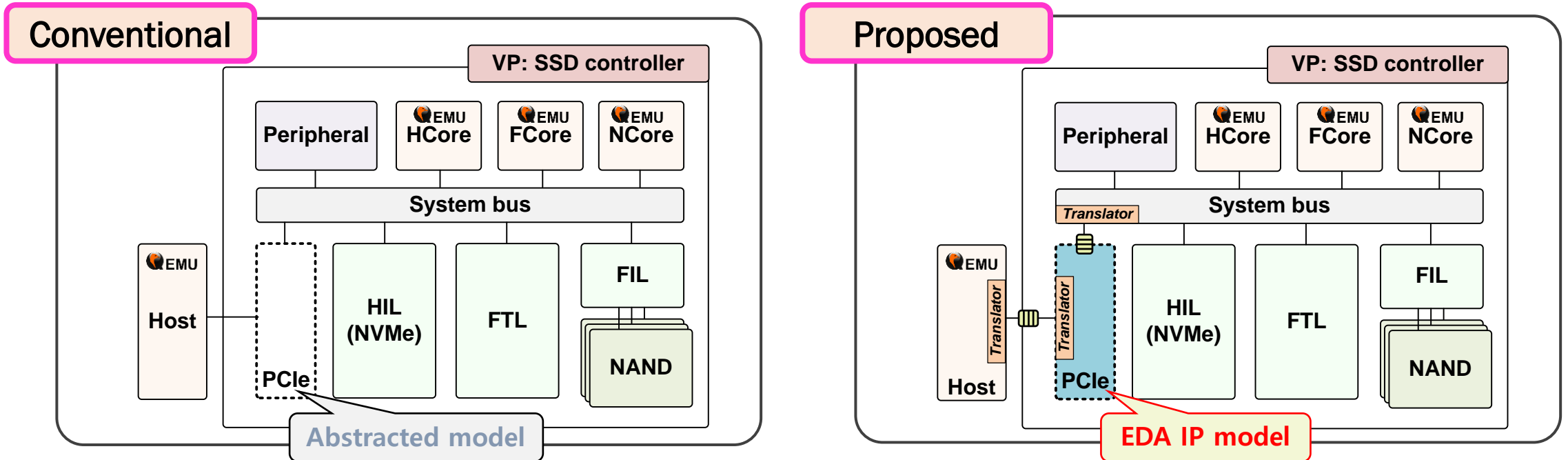
- **Solution #1:** With shared memory-based IPC method [2] at both interfaces, it is possible to synchronize between the two processes.

- ✓ When a sender needs to send a message, it increases the producer index (PI) in the shared memory.
- ✓ When the PI value changes are detected by the I/F of receiver, it reads the message and increases the value of consumer index (CI).
- ✓ After CI value being changed, each model continues its own tasks.

- **Solution #2:** Implementing packet translator for data format adjustment between the two models.

- ✓ **In VP,** receive the generic payload from EDA IP model and translate it to application-specific context and enroll the schedule.
- ✓ **In EDA IP model,** receive the application-specific context from VP-side and translate it to SystemC-TLM payload and notify an event to the scheduler of EDA IP model.

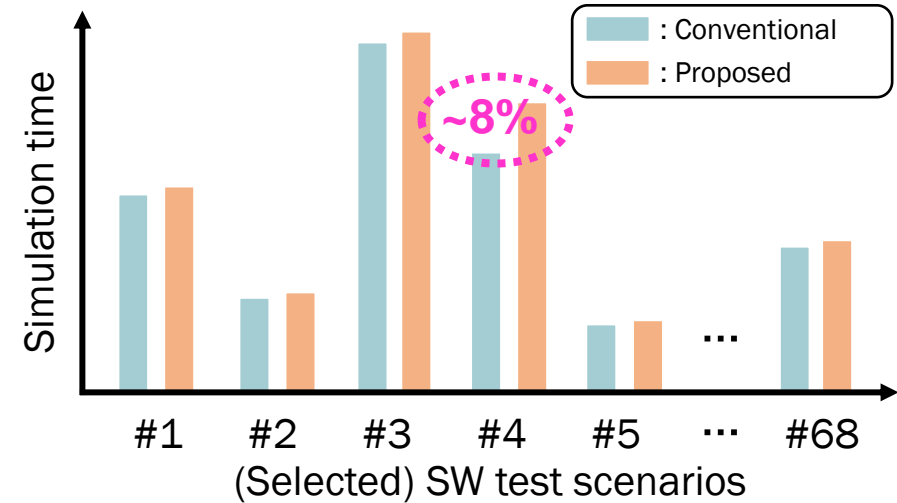
Practical Use: Our Case



- Conventional in-house VP had highly limited implementation of PCIe features.
- Therefore, it is impossible to accurately verify SW tests related to PCIe on the conventional In-house VP.
- By adding PCIe IP model provided by EDA vendor, it is possible to enhance the lacking features and increase functional accuracy of in-house VP.

Evidence

(All) SW test scenarios	Conventional	Proposed
Apple	✓	✓
Banana	✓	✓
Cherry	Not supported	✓
Dragon Fruit	Not supported	✓
Eggfruit	✓	✓
...
Zucchini	Not supported	✓



- Functional accuracy on the proposed VP has increased up to 100% while sacrificing the simulation performance up to 8%.
 - ✓ Functional accuracy: before: 63% → after: 100%, All TCs for product validation can be touched.
 - ✓ Simulation time of the proposed VP increased by up to 8 % (+ ~msecs). (*This is measured by using Flexible I/O (FIO) tester benchmark [3])
 - It is due to the shared memory IPC-based communication for accessing memory operations (R/W).
 - The increased simulation time does not have a significant impact on VP.

Summary

- The proposed work helps not only for shift-left of SW development, but also for improving SW quality through VP-based CI/CD because of the improvement of functional accuracy.
- We propose a method to improve functional accuracy of VP by exploiting EDA IPs.
 - The proposed method supports shared memory-based IPC to synchronize between the two model's simulations. It also translates data format from application-specific I/F (VP-side) into SystemC-TLM I/F (EDA IP-side), and vice-versa.
 - The experimental results show that the functional accuracy increases up to 100% with only a small fraction (8%) of the simulation time increase.

Thank you 😊

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Reference

- [1] K. Kang *et al.*, Seamless SoC verification using Virtual Platforms: An Industrial Case Study. DATE 2019
- [2] Sergio V. Tota *et al.*, MEDEA: a Hybrid Shared-memory/Message-passing Multiprocessor NoC-based Architecture. DATE 2010
- [3] “FIO: Flexible I/O Tester,” <http://linux.die.net/man/1/fio>.